REMARKS

In response to the Office Action of April 4, 2004, Applicant respectfully requests reconsideration. Claims 1-12 were previously pending in this application. By this amendment, Applicant is canceling claims 2 - 4 without prejudice or disclaimer. Claim 1 has been amended. As a result, claims 1 and 5-12 are pending for examination, with claim 1 being independent. No new matter has been added.

Rejections Under 35 U.S.C. §102 and §103

The Office Action has rejected claims 1-3 and 9-12 under 35 U.S.C. §102 as purportedly being anticipated by Higuchi et al, and claims 4-8 under 35 U.S.C. §103 as purportedly being obvious over Higuchi in view of Erickson. These rejections are respectfully traversed.

Claim 1 has been amended to incorporate the limitations of claims 2-4, such that claim 1 is now of the same scope as previously pending claim 4. As amended, claim 1 is directed towards error checking circuitry for performing error checks based on mathematical functions comprising a data input stage having a data node adapted to receive incoming data to be checked and a plurality of input feedback nodes, a register having a plurality of data input nodes each data input node being selectable to receive data from the data input stage and a set of output feedback nodes arranged to selectively supply a feedback signal to the data input stage, and multiplexing circuitry provided in association with the register and the data input stage to selectively connect one of said output feedback nodes to the data input stage and to selectively connect said data node to at least some of the said data input nodes such that the signal routes through the error checking circuitry are configurable to successively perform error checks based on different mathematical functions. The register comprises a plurality of delayed elements, each capable of holding one bit. The register further comprises a first data input node and a plurality of further data input nodes disposed between selected ones of the delay elements. The multiplexing circuitry is arranged to selectively connect an incoming data signal from the input stage and a zero signal to said data input nodes of the register.

As mentioned above, claim 1 is commensurate in scope with previously pending claim 4, which was rejected under §103 as purportedly being obvious over Higuchi and Erickson. The

Office Action concedes that Higuchi does not disclose multiplexing circuitry used to input a zero signal to the data input node but asserts Erickson teaches multiplexing circuitry that selects between an input signal and a zero signal to be connected to the input signal of the register. Based on that, the Office Action asserts that it would have been obvious to one skilled in the art to modify the device of Higuchi to employ multiplexing circuitry that selects between an input signal and a zero signal to be connected to the input signal of the register. Applicant respectfully disagrees.

Higuchi

Higuchi discloses a CRC generating circuit for generating a cycle code that is added to transmission data for error monitoring, and specifically relates to a variable CRC generating circuit in which the number of stages of the CRC can be arbitrarily varied ([0001]). As seen in Figure 1 (relied upon in the Office Action), the device disclosed by Higuchi contains an input stage consisting of an AND gate 20 and an EXCLUSIVE OR gate 11_0 which non-selectively supplies the N-1 stages of unit arithmetic circuits with the data to be corrected ([0009]).

Erickson

Erickson discloses a method for generating a long error checking polynomial remainder having the ability to detect errors with high reliability and inserting only a subset of the polynomial remainder periodically into a data stream (Abstract). Figure 6 (relied upon in the Office Action) discloses a circuit which is capable of selectively transmitting a logic zero input or a value CRCIN into an EXCLUSIVE OR gate.

No Motivation Is Provided For the Combination

The Office Action alleges that one of the skill in the art would have been motivated to employ the multiplexing circuitry of Erickson in place of the multiplexing circuitry of Higuchi "because the two circuits are functional the same providing same result for the same purpose." (Office Action, page 5). Nothing in Erickson, Higuchi or any other prior art reference of record is cited to support this assertion, such that the assertion appears to be based entirely on the improper use of hindsight. For example, the Office Action does not point to any teaching in

either reference that would suggest that one skilled in the art would have considered the circuits to perform the same function, let alone provide motivation for one skilled in the art to modify the Higuchi circuit for any purpose. Thus, it is respectfully asserted that the combination of Higuchi and Erickson under §103 is improper, and that claim 1 patentably distinguishes over the prior art of record. Claims 5-12 depend from claim 1 and are patentable for at least the same reasons.

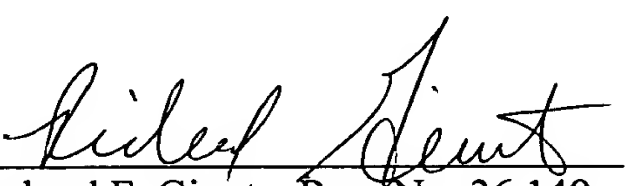
CONCLUSION

In view of the foregoing, the application is believed to be in condition for allowance. A notice to this effect is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication is not believed to place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,

Rodrigo Corder

By: 

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